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DATE MAILED: 06/17/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/829,053	04/21/2004	Sanjeev Aggarwal	TI 35817	6820	
23494 7:	590 06/17/2005	EXAMINER			
TEXAS INST	RUMENTS INCOR	CHAUDHARI,	CHAUDHARI, CHANDRA P		
P O BOX 6554	74, M/S 3999				
DALLAS, TX	75265	ART UNIT	PAPER NUMBER		
			2891		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applicatio	n No.	Applicant(s)			
Office Action Summary		10/829,05	3	AGGARWAL ET AL.			
		Examiner		Art Unit			
		Chandra C		2891			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply sepecified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1)⊠	Responsive to communication(s) filed on	28 March 2005.					
2a)	This action is <b>FINAL</b> . 2b)	☐ This action is no	on-final.				
3) 🗌	Since this application is in condition for allowance except for formal matters, prosecution as to the ments is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
5)	<u> </u>						
Applicat	ion Papers						
9)[	The specification is objected to by the Ex	aminer.					
10)⊠ The drawing(s) filed on <u>21 April 2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.							
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority (	ınder 35 U.S.C. § 119						
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>							
2) Notice 3) Infor	et <b>(s)</b> se of References Cited (PTO-892) se of Draftsperson's Patent Drawing Review (PTO-9 mation Disclosure Statement(s) (PTO-1449 or PTO- er No(s)/Mail Date <u>April 21, 2004</u> .		4) Interview Summar Paper No(s)/Mail I 5) Notice of Informal 6) Other:	ry (PTO-413) Date I Patent Application (PT0	0-152)		

Application/Control Number: 10/829,053

Art Unit: 2891

Applicant's election without traverse of claims 1-13, 17-32 in the reply filed on March 28, 2005 is acknowledged.

Claims 30-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 30, lines 7-8, "the planarized ferroelectric dielectric layer" lacks antecedent basis;

line 9, "planarizing" should be "planarized".

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 5-7, 12-13, 17-18, 21-23, 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagata – US 6,232,174.

Nagata (Figs. 2A-2F and text in col. 4, lines 2-64, and col. 8, line 41 to col. 9, line 62) discloses the claimed invention by manufacturing a ferroelectric random access memory by forming a transistor with source/drain regions 4, interlevel dielectric 5 with conductive plug 6, 1st electrode 7, forming 2nd electrode 11 over the planarized (using CMP) and cleaned ferroelectric dielectric layer 8.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4, 8-11, 19-20, 24-27, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata and Gilbert – US 2001/0044205.

Nagata is applied as above and does not disclose the average surface roughness of the ferroelectric dielectric layer, nor planarizing at least a portion of the 2nd electrode layer prior to forming the 2nd protective layer, nor cleaning the planarized 1st electrode layer prior to forming the ferroelectric dielectric layer. Gilbert (Fig.1 and text in paragraphs 17-20, 38-47, and 96) teaches that a planar capacitor is more uniform, and economizes on process time and cost. Cleaning is necessary to reduce leakage current. Nagata has already disclosed that the 2nd electrode layer is cleaned prior to forming the 2nd protective layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to planarize as taught by Gilbert in Nagata's process to economize on process time and cost, and clean and planarize the 1st electrode layer to reduce leakage current. One may reasonably use CMP to planarize the ferroelectric dielectric layer to attain the claimed average surface roughness to reduce cell size and capacitor leakage current.

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Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Chandra Chaudhari whose telephone number is 571-272-1688. The examiner

can normally be reached on Mon - Fri (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill

Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this

application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be obtained

from either Private PAIR or Public PAIR. Status information for unpublished applications is available

through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the

Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chandra Chaudhari

**Primary Examiner** 

Art Unit 2891

C Chaudhari Chandra Chaudhari

June 10, 2005